



Pico Computing Demonstrates Bioinformatics Acceleration at SC 2011

Pico's SC5 FPGA cluster reduces short read sequencing from 6 ½ hours to just one minute

Seattle, WA – November 9, 2011 – Pico Computing will be demonstrating an FPGA implementation of BFAST resulting in a 350X acceleration over a software-only implementation running on two quad core Intel Xeon processors. The 350X acceleration was achieved using 8 Pico M-503 FPGA modules in their SC5 SuperCluster chassis. The BFAST algorithm is primarily used in short read genome mapping.

The study of DNA has become computationally intensive to due to rapid improvements in both cost and throughput of next-generation sequencing machines. Scientists use these next-generation sequencing machines to replicate a DNA strand many times, randomly cut strands into short lengths, sequence the nucleotide bases of each length, and then compare against a known reference genome.

Next-generation sequencing machines are able to sequence the short pieces of DNA, which are called short reads, in a massively parallel fashion, leading to lower cost per genome and higher throughput per run. However, the process of mapping those short reads to a reference genome relies on software programs to search the three billion base-pair genome for places where each short read appears. The time required to complete this mapping phase is becoming the bottleneck for DNA studies, since CPUs are not able to exploit the inherent data parallelism in the search.

The BFAST algorithm finds possible match locations for each short read in the genome and then Smith-Waterman is used to score each location. "FPGAs offer the potential for drastic improvement in the runtime of the mapping phase because we can greatly accelerate this searching process," said Corey Olson, Senior Engineer at Pico Computing and developer of the BFAST implementation. "With a scalable FPGA system such as the M-503, we accelerate both the process of finding candidate alignment locations and the Smith-Waterman scoring."

Pico Computing will be demonstrating the FPGA BFAST implementation at Supercomputing 2011 (SC11) November 14-18, 2011 in Seattle, Washington (booth #2300). In addition, Corey Olson will be giving a talk during SC11, titled: "FPGA Acceleration of Short Read Human Genome Mapping" at 4:30pm on Tuesday, November 15th in room WSCC 613/614.

About Pico Computing

Pico Computing, headquartered in Seattle, Washington, specializes in highly integrated development and deployment platforms based on Field Programmable Gate Array (FPGA) technologies. Applications for Pico Computing technologies include cryptography, networking, signal processing, bioinformatics, and scientific computing. Pico Computing products are used in embedded systems as well as in military, national security and high performance computing applications. For more information about Pico products and services, visit www.picocomputing.com.

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Shown with three M-503 FPGA Modules