

**PICO COMPUTING INC.**

**PICO E-12**  
**HARDWARE TECHNICAL**  
**REFERENCE**

Release: 3.1.6.02  
Hardware Version: C



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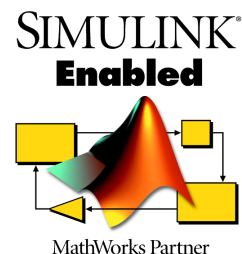
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## Product Overview:

The PICO family of products are revolutionary embedded platforms. With performance that often exceeds modern microcomputers, a shockingly small form factor, and nominal power consumption that is less than one watt, the PICO family of products take computing to a whole new level.

The PICO E-12 is based on the revolutionary Virtex-4 chip. This device has the performance and power consumption of a custom chip (ASIC), but is completely reconfigurable! There are two versions of the PICO E-12; “Logic Optimized” (LO) and “Embedded Processor” (EP). The Logic Optimized versions offer the most user configurable logic, while the embedded processor version trades off some gates for an embedded Power-PC™ processor.

Advanced users will enjoy the open source development kits which allow absolute control over the hardware. Those who desire a high level programming environment can use Simulink® to implement custom algorithms in hardware with just the click of a button. Impulse C™ support is also included for rapid firmware development in the C programming language. Board support packages are available for operating systems such as Linux or  $\mu$ C/OS.



## PICO E-12 Quick Reference Datasheet

### FEATURES

- ◆ High-performance Virtex-4 FX-12 or LX-25
- ◆ 128 MB RAM
- ◆ 64 MB Flash ROM
- ◆ Compact flash interface
- ◆ Open source
- ◆ Standalone operation
- ◆ Reconfigurable, high speed digital bus

### FPGA FEATURES

- ◆ Embedded PowerPC™ P405 processor
- ◆ Integrated DSP logic

### APPLICATIONS

- ◆ Simulink acceleration
- ◆ Impulse C™ Platform
- ◆ Embedded Systems
- ◆ Digital signal processing
- ◆ Encryption / decryption
- ◆ Software defined radio
- ◆ Image processing
- ◆ Communications protocol decoding
- ◆ Supercomputing / Cluster computing

### IO MODULES

- ◆ 10/100/1000 Ethernet
- ◆ RS-232 Asynchronous Serial
- ◆ RS-422/485 Asynchronous Serial
- ◆ RS-232 Synchronous Serial
- ◆ Full Speed USB
- ◆ CAN Bus
- ◆ High Power Relay Control
- ◆ Analog In
- ◆ Analog Out
- ◆ Audio In
- ◆ Audio Out
- ◆ JTAG

### MECHANICAL

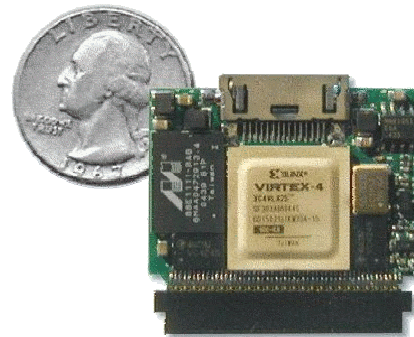
Temperature Range: -40°C\* to +85°C  
Compact Flash Type II form factor  
Stainless steel case

### POWER

Minimum: 0.4W  
Nominal: 0.75W  
Absolute Maximum: 4.95W  
Supply Voltage: 3.15 – 5.25V

### FPGA PERFORMANCE

18x18 Multiply – 48 Billion / Second  
DES – 400M Keys / Second  
MD4 – 100M Keys / Second



E-12 Card

\*Operation below -20°C requires throttled RAM timings

## PICO E-12 Electrical Specifications



	<b>Minimum</b>	<b>Nominal</b>	<b>Maximum</b>
DC Input Voltage	3.15V	3.3V - 5.0V	5.5V
Power Consumption	0.4W	0.5W	4.5W
DC Input Current	0.08A	0.12A	1.5A
Recommended Temperature Range	-20°C	10°C	70°C
Maximum Allowable Temperature Range	-40°C*		85°C
Continuous Storage Temperature Range	-50°C	30°C	90°C
Relative Humidity (Non-Condensing)	0%		95%

\*Operation below -20°C requires throttled RAM timings

# System Architecture



At the core of the PICO E-12 is a Virtex-4 FPGA. The FPGA can be dynamically configured to perform any number of specialized tasks such as: protocol processing, encryption, or complex mathematical functions. Embedded systems benefit from the integrated Power-PC™ processor available on the EP series cards.

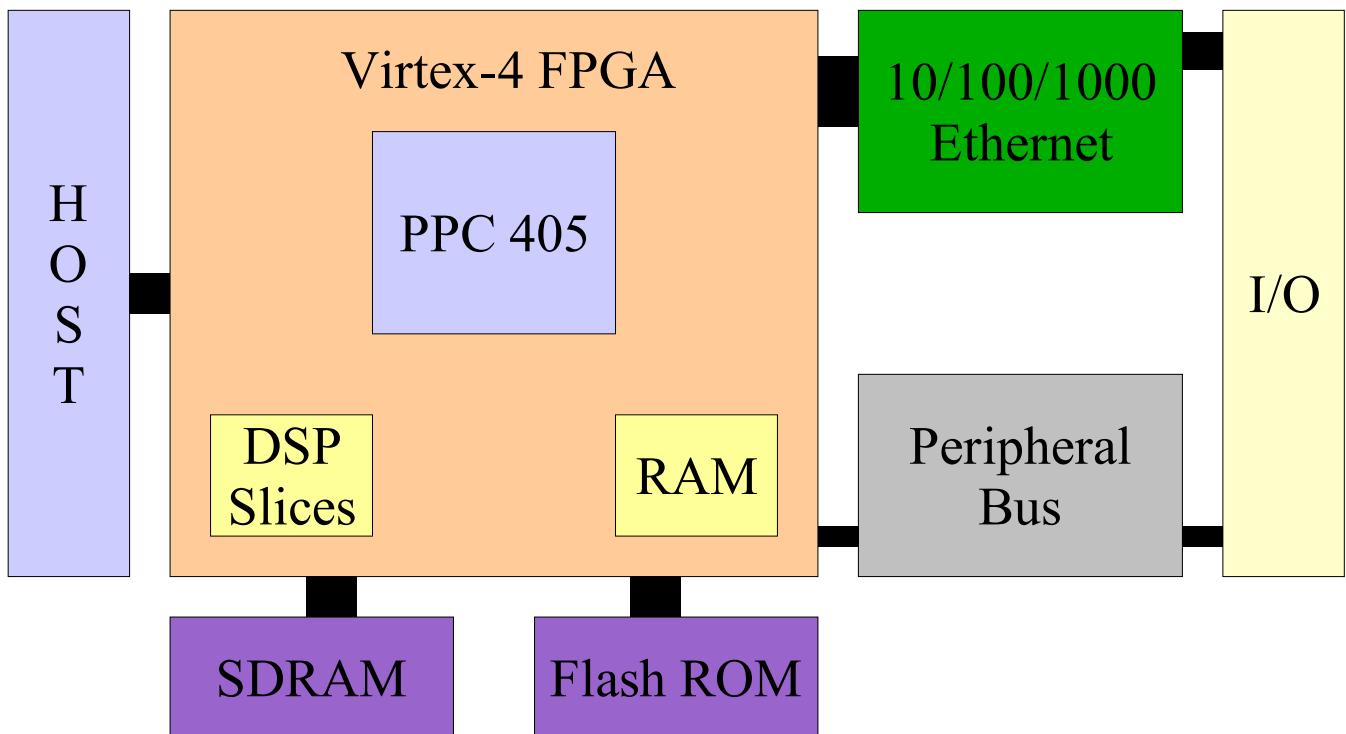


Figure 1

## Field Programmable Gate Array



The core of the PICO E-12 is a high performance Virtex-4 FPGA. Included in the FPGA are the FPGA Fabric, an optional Power-PC™ processor, ultra high-speed DSP slices and RAM.

### FPGA Fabric:


The “Fabric” of an FPGA comprises an array of logic elements that can be connected in virtually unlimited patterns. These patterns of logic elements can be used to perform basic mathematical functions such as addition and subtraction, or can be grouped together to perform complex functions like Fast Fourier Transforms. Logic elements can even be connected to create a custom soft processor.

The advantage of the FPGA is that the internal logic can be optimized for a specific application. FPGAs are also able to execute operations in parallel, not being limited by sequential execution like a traditional processor. FPGA operations can be executed in a parallel, pipelined or even an asynchronous manner. The FPGA allows incredible application speed with very low power consumption. Your imagination is really the limit.

### DSP Slice:

Embedded within the FPGA are special areas that are designed to facilitate high speed “digital signal processing.” These areas are called DSP slices. The DSP slice can be configured in a variety of different ways. For example one DSP slice can be configured to be one tap of an FIR filter. DSP slices are fully pipelined and feature incredible speed. When configured for FIR filtering the DSP slice has a guaranteed performance of 500MHz with a latency of one cycle. An 18x18 multiply and accumulate also runs at 250MHz with a latency of two cycles. Smaller data widths allow higher clock speeds.

### FPGA Resources:

Free FPGA Cores	<a href="http://www.opencores.org">www.opencores.org</a>	repository of free, open source IP cores	 <b>OPENCORES.ORG</b>	
Virtex-4 Website	<a href="http://www.xilinx.com/virtex4">www.xilinx.com/virtex4</a>			

# PowerPC™ Processor



## PPC405x3 Processor Introduction:

FPGAs are renowned for their ability to process parallel logic, but they typically have a hard time emulating a high performance processor. To get the best of both worlds the Virtex-4™ features an embedded Power PC Processor. Since the processor shares the same die as the FPGA it seamlessly interfaces with the FPGA fabric.

A new feature of the Vitex-4 FPGA is the addition of an auxiliary processor interface. The APU is the highest speed interface between the Power-PC™ processor and the FPGA fabric. Up to four custom instructions may be implemented in the FPGA, which are accessible from the Power-PC™.

Board support packages are currently available for  $\mu$ C/OS and Linux. Board support source code is available open source under the GPL.

## CPLD TurboLoader



A CPLD (Complex Programmable Logic Device) is a smaller version of an FPGA (described above) with permanent Flash storage built in. The PICO E-12 contains one CPLD that loads and reconfigures the FPGA. The CPLD can also place the FPGA in a low power sleep mode. The PICO firmware guide describes how to access the CPLD Image Manager.

### CPLD Resources:

Xilinx CPLD Website	<a href="http://www.xilinx.com/cpld">www.xilinx.com/cpld</a>
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## Tri-Mode Ethernet Interface



The PICO E-12 features the Marvell Alaska series 88E1111 tri-mode Ethernet transceiver. On EP series parts the MAC (Middle access controller) is implemented on the FPGA die. On LO series parts the MAC must be implemented in firmware. Communication between the MAC and PHY takes place over an industry standard MII/GMII interface.

The Ethernet transceiver features 10/100/1000 full/half duplex operation. It will automatically configure the physical interface on the fly for crossover or straight through operation. The PHY can even automatically correct for common wiring mistakes. The PHY has a built in Time Domain Reflectometer which can diagnose cable problems and pinpoint their distance away from the transceiver.

The Ethernet interface on the PICO is magnetic-less allowing high speed, low power digital interconnect directly to Ethernet backplanes. DO NOT directly connect the Ethernet interface to a hub or switch without a magnetic isolation module.

The Marvell 88E1111 is the only chip on the PICO E-12 that requires an NDA for access to the datasheets. If you are interested in some of the advanced features not supported by the native driver, contact PICO Computing for assistance in obtaining an NDA from Marvell. Users are warned not to contact Marvell directly.

### Ethernet Resources:

Marvell 88E1111 Webpage	<a href="http://www.marvell.com/products/transceivers/singleport/88e1111.jsp">http://www.marvell.com/products/transceivers/singleport/88e1111.jsp</a>
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# Flash Memory



The PICO E-12 comes equipped with at least 64 megabytes of Flash ROM. The Flash ROM is divided into 512 sectors that can be erased independently. Most of the space on the ROM is reserved for the user.

The Flash ROM's address bus can be controlled by either the TurboLoader or the FPGA (but not both). During power-up or reboot, the TurboLoader is in control of the Flash ROM Address bus. At all other times the FPGA is in control of the address bus.

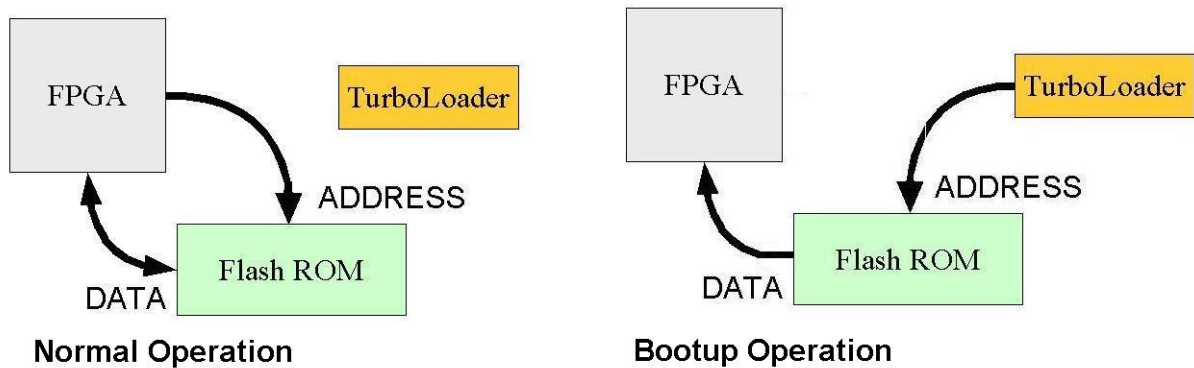


Figure 2

## Typical Flash ROM Allocation Table:

Byte addresses	Description	Flash Sectors
0x00000000-0x0000FFFF	Tuple Data and configuration management	0
0x00010000-0x0006FFFF	Primary FPGA Image	1-6
0x000A0000-0x000FFFFFFF	Backup FPGA Image	7-12
0x000D0000-0x0012FFFF	Secondary Image including boot loader	13-19
0x00140000-0x01FFFFFFF	Other FPGA images, executables and data files	20-511

The Flash ROM has a simple, open file system which allows the user to store FPGA images, ELF binary files, or other data. The primary image is used to boot the FPGA initially, and the backup image is only invoked if the primary image fails to load correctly. Executable files are in ELF format and are loaded by a loader within the secondary image. The primary image will either load the secondary image or pause for the PC to access and manage the file system.

# SDRAM Memory



The PICO E-12 comes equipped with 128 MB of PC-133 SDRAM memory. There are two 256Mb chips both with a 16 bit data path that is grouped into one 32 bit bank. From -20°C to +85°C, the ram can run at 133 MHz. For operation at temperatures below -20°C, special firmware with reduced ram timings is required. The temperature compensated self-refresh mode must be disabled below -20°C.

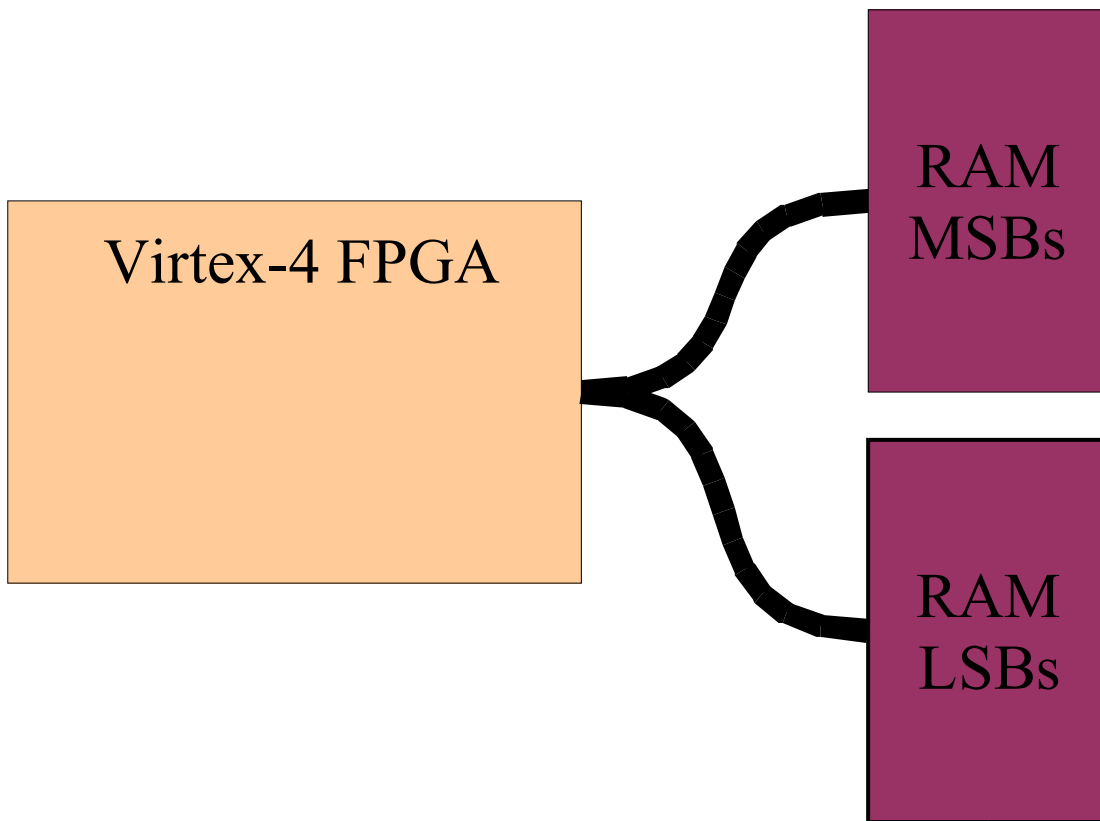


Figure 3

## Digital Peripheral Interface

The PICO E-12 features 4 GPIO lines which are used for external peripheral support. The GPIO lines are enabled when the external DIAG\_EN pin is left floating or pulled up to 2.5V. Pulling the DIAG\_EN pin low replaces all GPIO signals with JTAG signals.

All GPIO signals have user selectable pull-up, pull-down, keeper or HI-Z termination. Drive strength is also user selectable between 2 and 24mA. All GPIOs can be configured for input, output and bi-directional mode.

<b>DIAG_EN State</b>	<b>JTAG</b>	<b>GPIO</b>
Float / High	Disabled	Enabled
Low	Enabled	Disabled

<b>Electrical Specifications</b>	<b>Minimum</b>	<b>Nominal</b>	<b>Maximum</b>
High Voltage	1.7V	2.5V	2.9V
Low Voltage	-0.2V	0V	0.7
Input Impedance (Pulldowns Disabled)		HI-Z	
Drive Strength (Selectable)	2 mA		24 mA
ESD Withstand Voltage (Human Body Model)			2 KV

## Compact Flash Interface



The PICO E-12 can run as a standalone product or be connected to a host using the compact flash connector. By default, the Pico E-12 ships with firmware that is ready for use as a compact flash device.

The Compact Flash interface is a subset of PCMCIA. The data path is 16 bits wide and is asynchronous. Compact Flash is compatible with all Cardbus and PCMCIA based systems. The wiring of the compact flash interface supports memory, IO and DMA transfers.

Since compact flash systems can be either 3.3V or 5V digital translating transceivers are required to connect with a host. There are three transceivers on the PICO E-12 which can have their direction controlled independently. With this innovative design it is actually possible to reverse the CF interface and use the PICO E-12 as a host controller. The transceivers are so flexible that they can be connected to just about any digital bus that runs anywhere between 3.3 and 5 volts.

Those who are interested in alternate interfaces should contact PICO Computing. The PCMCIA decoder source code and support is available.

### PCMCIA Interface Resources:

CompactFlash Association	<a href="http://www.compactflash.org">www.compactflash.org</a>
PCMCIA Website	<a href="http://www.pcmcia.org">www.pcmcia.org</a>

## Digital Bus Interface



When the PICO E-12 is not connected to a compact flash host, the digital bus can be reconfigured to connect with a wide variety of high speed digital busses and peripherals. The digital bus is divided into four groups (control, address, low data and high data). Each one of these groups can be configured as an input or output group (direction can be changed on the fly). With proper external termination speeds of over 100 MHz are possible. The external digital bus is set to transmit and receive at the external supply voltage of the PICO E-12 which allows connectivity to both 3.3V and 5V systems.

Net	Description	Safe State
CF_MASTER_EN	Master enable for the compact flash bus	High (Interface disabled)
CF_ADDRESSDIR	Address and status line direction	Low (Driven by host)
CF_CTRLDIR	Control line direction	High (Driven by PICO)
CF_DATADIR_H	Databus direction bits [6-15]	Low (Driven by host)
CF_DATADIR_L	Databus direction bits [0-7]	Low (Driven by host)

### Signal Group

CF_CTRLDIR	CF_ADDRESSDIR	CF_DATADIR_L	CF_DATADIR_H
CF_BVD1	C\F\ \C\E1\	CF_D0	CF_D8
CF_BVD2	C\F\ \C\E2\	CF_D1	CF_D9
C\F\ \I\N\PA\C\	C\F\ \R\E\G\	CF_D2	CF_D10
CF_WP	C\F\ \O\E\	CF_D3	CF_D11
C\F\ \W\A\I\T\	C\F\ \W\E\	CF_D4	CF_D12
CF_READY	C\F\ \I\O\R\D\	CF_D5	CF_D13
	C\F\ \I\O\W\R\	CF_D6	CF_D14
	C\F\ \C\S\E\L\	CF_D7	CF_D15
	CF_RESET		
	CF_READY		
	CF_A0		
	CF_A1		
	CF_A2		
	CF_A3		
	CF_A4		
	CF_A5		
	CF_A6		
	CF_A7		
	CF_A8		
	CF_A9		
	CF_A10		

<b>Direction Control Lines</b>	
High	Signal Driven by PICO [Output]
Low	Signal Driven by Host [Input]

<b>Electrical Specifications (DC)</b>	<b>Minimum</b>	<b>Nominal</b>	<b>Maximum</b>
Positive Supply Input Voltage (Vcc)	3.15V	5.0V	5.5V
Low Level Input Voltage	0V	0V	0.7V
High Level Input Voltage	2V	Vcc	Vcc
Drive Strength		24mA	
Input Impedance		HI-Z	
Internal Bus Voltage		3.0V	

**For more information on the transceivers obtain a datasheet from:**

<a href="http://www.ti.com">www.ti.com</a>	Search for: SN74ALVC164245KR
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## JTAG Debug Interface



The PICO E-12 is equipped with a JTAG diagnostic port which allows real-time debugging of hardware, firmware and software. Use of the external JTAG port disables all external GPIO as well as the internal JTAG loop back.

Some JTAG programs require the length of the instruction register (IR). The IR length is listed below for all devices in the JTAG chain.

Device	Instruction register bit length
FPGA	10
Optional Power-PC™	10
TurboLoader	8
Ethernet PHY	8

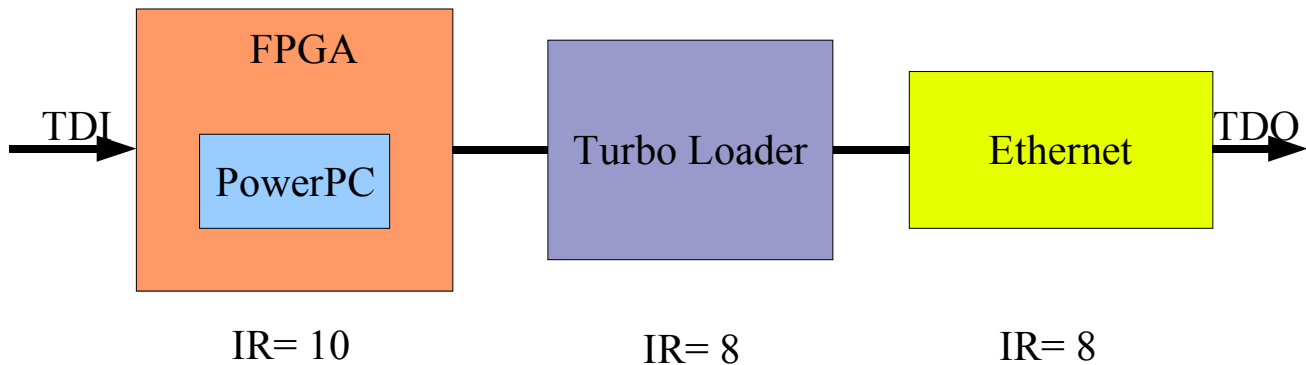


Figure 4

The Primary Image in the Flash ROM contains an embedded JTAG diagnostic port. This allows a user in Windows or Linux to debug software without an external JTAG cable. The internal JTAG diagnostic loop back looks just like a Parallel Port IV diagnostic cable when used with the PICO E-12 driver.

## Appendix A – Peripheral I/O Connector Information

### Connector Information

Description	Brand	Part Number
Mating Connector	Honda	RMC-E15FB-BSLAN-MA13

\*Connectors are always in stock at PICO Computing

### Peripheral I/O Connector Pinout

1	ETHER_OUT_D-	Digital Ethernet <b>DO NOT CONNECT DIRECTLY TO EXTERNAL DEVICES</b>
2	ETHER_OUT_D+	Digital Ethernet <b>DO NOT CONNECT DIRECTLY TO EXTERNAL DEVICES</b>
3	ETHER_OUT_C-	Digital Ethernet <b>DO NOT CONNECT DIRECTLY TO EXTERNAL DEVICES</b>
4	ETHER_OUT_C+	Digital Ethernet <b>DO NOT CONNECT DIRECTLY TO EXTERNAL DEVICES</b>
5	ETHER_OUT_B-	Digital Ethernet <b>DO NOT CONNECT DIRECTLY TO EXTERNAL DEVICES</b>
6	ETHER_OUT_B+	Digital Ethernet <b>DO NOT CONNECT DIRECTLY TO EXTERNAL DEVICES</b>
7	ETHER_OUT_A-	Digital Ethernet <b>DO NOT CONNECT DIRECTLY TO EXTERNAL DEVICES</b>
8	ETHER_OUT_A+	Digital Ethernet <b>DO NOT CONNECT DIRECTLY TO EXTERNAL DEVICES</b>
9	2.5V	2.5V 0.45A peripheral power
10	GPIO-4 / TMS	General purpose I/O 4 or JTAG TMS
11	GPIO-3 / TCK	General purpose I/O 3 or JTAG TCK
12	GPIO-2 / TDO	General purpose I/O 2 or JTAG TDO
13	GPIO-1 / TDI	General purpose I/O 1 or JTAG TDI
14	DIAG_EN	JTAG port enable when shorted to ground
15	GND	Ground return

### Peripheral Connector Pin #1 Location

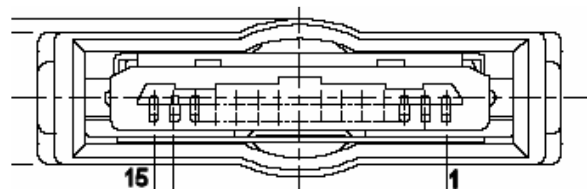


Figure 5

## Appendix B – Compact Flash Connector Information

### Connector Information

Description	Brand	Part Number
CF Header	Hirose	MI20-50PD-SF
CF Header	Samtec	CFT-125-02-L-D-RA-01-SL

The Pico E-12 will mate with any Type-II Compact Flash Header

The function and direction of the pins on the Compact Flash interface can be easily changed. Please see the “Digital Bus Interface” section for more information.

### Compact Flash Connector Pinout

Name	Pin	Description	Dir
GND	1	Card Ground	N/A
D3	2	Bidirectional Data Line 3	I/O
D4	3	Bidirectional Data Line 4	I/O
D5	4	Bidirectional Data Line 5	I/O
D6	5	Bidirectional Data Line 6	I/O
D7	6	Bidirectional Data Line 7	I/O
-CE1	7	Card Enable 1	I
A10	8	Address Line 10 [MSB]	I
-OE	9	Output Enable (Memory Transfer)	I
A9	10	Address Line 9	I
A8	11	Address Line 8	I
A7	12	Address Line 7	I
VCC	13	Card Power (Sets Compact Flash Inteace Voltage)	N/A
A6	14	Address Line 6	I
A5	15	Address Line 5	I
A4	16	Address Line 4	I
A3	17	Address Line 3	I
A2	18	Address Line 2	I
A1	19	Address Line 1	I
A0	20	Address Line 0 [LSB]	I
D0	21	Bidirectional Data Line 0 [LSB]	I/O
D1	22	Bidirectional Data Line 1	I/O
D2	23	Bidirectional Data Line 2	I/O
WP	24	Write Protect	O
GND	25	Card Ground	N/A
-CD1	26	Card Detect 1 (Grounded Internally)	O
D11	27	Bidirectional Data Line 11	I/O
D12	28	Bidirectional Data Line 12	I/O
D13	29	Bidirectional Data Line 13	I/O
D14	30	Bidirectional Data Line 14	I/O
D15	31	Bidirectional Data Line 15 [MSB]	I/O
-CE2	32	Card Enable 2	I
GND	33	Card Ground	N/A

-IORD	34	I/O Read	I
-IOWR	35	I/O Write	I
-WE	36	Write Enable (Memory Transfer)	I
READY	37	IRQ	O
VCC	38	Card Power (Sets Compact Flash Interface Voltage	N/A
-CSEL	39	Master/Slave Select	I
-VS2	40	Voltage Select 2	O
RESET	41	Card Master Reset	I
-WAIT	42	Cycle Extension Request	O
-INPACK	43	I/O Input Acknowledge	O
-REG	44	Attribute Memory Transfer	I
BVD2	45	Battery Voltage Detect 1	O
BVD1	46	Battery Voltage Detect 2	O
D8	47	Bidirectional Data Line	I/O
D9	48	Bidirectional Data Line	I/O
D10	49	Bidirectional Data Line	I/O
GND	50	Card Ground	N/A

## Compact Flash Connector Pull Up and Pull Down Information

Name	Pin	Description	Value
-CE1	7	Pull Up	280K
-CE2	32	Pull Up	280K
-REG	44	Pull Up	280K
-IOWR	35	Pull Up	280K
-IORD	34	Pull Up	280K
READY	37	Pull Up	280K
-INPACK	43	Pull Up	280K
-WAIT	42	Pull Down	280K

For additional information consult the free Compact Flash Standard available from:  
[www.compactflash.org](http://www.compactflash.org).

## Appendix C – FPGA Pinout

### FPGA Pinout

Name	Pin	Description	Dir	I/O Standard
50MHZ_CLOCK	Y9	50 MHz Clock In +/- 50 ppm - Internal Pull Down Required	I	LVTTTL
50MHZ_CLOCK	W10	50 MHz Clock In +/- 50 ppm [Slave Clock – Do not Use]	I	LVTTTL
50MHZ_CLOCK	W11	50 MHz Clock In +/- 50 ppm	I	LVTTTL
50MHZ_CLOCK	Y11	50 MHz Clock In +/- 50 ppm [Slave Clock – Do not Use]	I	LVTTTL
50MHZ_CLOCK	Y12	50 MHz Clock In +/- 50 ppm	I	LVTTTL
50MHZ_CLOCK	W13	50 MHz Clock In +/- 50 ppm - Internal Pull Down Required	I	LVTTTL
C\F\ \C\E\1\	T6	Card Enable #1 [LSBs]	I	LV_TTL 3.3V
C\F\ \C\E\2\	U4	Card Enable #2 [MSBs]	I	LV_TTL 3.3V
C\F\ \C\S\E\L\	R4	Master/Slave Select	I	LV_TTL 3.3V
C\F\ \I\N\P\A\C\	Y6	I/O Input Acknowledge	I	LVTTTL
C\F\ \I\O\R\I\	W3	I/O Read from Card	I	LV_TTL 3.3V
C\F\ \I\O\W\R\	U5	I/O Write to Card	I	LV_TTL 3.3V
C\F\ \O\E\	V4	Memory Read from Card	I	LV_TTL 3.3V
C\F\ \W\A\I\T\	W8	CF Extend Read Cycle	O	LVTTTL
C\F\ \W\E\	U3	Memory Write to Card	I	LV_TTL 3.3V
C\F\ \R\E\I\G\	T2	Attribute Memory Access	I	LV_TTL 3.3V
CF_A0	R2	Address Line 0 [LSB]	I	LV_TTL 3.3V
CF_A1	U2	Address Line 1	I	LV_TTL 3.3V
CF_A2	V1	Address Line 2	I	LV_TTL 3.3V
CF_A3	W2	Address Line 3	I	LV_TTL 3.3V
CF_A4	T1	Address Line 4	I	LV_TTL 3.3V
CF_A5	R1	Address Line 5	I	LV_TTL 3.3V
CF_A6	T4	Address Line 6	I	LV_TTL 3.3V
CF_A7	T3	Address Line 7	I	LV_TTL 3.3V
CF_A8	W4	Address Line 8	I	LV_TTL 3.3V
CF_A9	U6	Address Line 9	I	LV_TTL 3.3V
CF_A10	W5	Address Line 10 [MSB]	I	LVTTTL
CF_ADDRESSDIR	Y4	Address Direction	O	LV_TTL 3.3V
CF_BVD1	Y7	Battery Voltage Detect #1	O	LVTTTL
CF_BVD2	W7	Battery Voltage Detect #2	O	LVTTTL
CF_CTRLDIR	V3	Control Line Direction	O	LV_TTL 3.3V
CF_D0	T17	Data Line 0 [LSB]	I/O	LV_TTL 3.3V
CF_D1	T18	Data Line 1	I/O	LV_TTL 3.3V
CF_D2	U18	Data Line 2	I/O	LV_TTL 3.3V
CF_D3	R20	Data Line 3	I/O	LV_TTL 3.3V
CF_D4	V19	Data Line 4	I/O	LV_TTL 3.3V
CF_D5	T20	Data Line 5	I/O	LV_TTL 3.3V
CF_D6	U17	Data Line 6	I/O	LV_TTL 3.3V
CF_D7	T19	Data Line 7	I/O	LV_TTL 3.3V
CF_D8	U19	Data Line 8	I/O	LV_TTL 3.3V
CF_D9	V18	Data Line 9	I/O	LV_TTL 3.3V
CF_D10	V17	Data Line 10	I/O	LV_TTL 3.3V
CF_D11	W17	Data Line 11	I/O	LV_TTL 3.3V

CF_D12	Y17	Data Line 12	I/O	LV_TTL 3.3V
CF_D13	W19	Data Line 13	I/O	LV_TTL 3.3V
CF_D14	V20	Data Line 14	I/O	LV_TTL 3.3V
CF_D15	W18	Data Line 15 (16 Bit Mode) / Address Line -1 (8 Bit Mode)	I/O	LV_TTL 3.3V
CF_DATADIR_H	R18	Data Direction [MSBs]	O	LV_TTL 3.3V
CF_DATADIR_L	R19	Data Direction [LSBs]	O	LV_TTL 3.3V
CF_MASTER_EN	R3	Compact Flash Master Enable	O	LV_TTL 3.3V
CF_READY	W6	IRQ	O	LVTTTL
CF_RESET	V2	Reset	I	LV_TTL 3.3V
CF_WP	Y5	Write Protect	I	LVTTTL
ETHER_25MHZ	F3	25 MHz Clock	O	LV_CMOS 2.5V
ETHER_125MHZ	H1	125 MHz Clock	I	LV_CMOS 2.5V
ETHER_125MHZ	W9	125 MHz Clock	I	LVTTTL
ETHER_COL	P4	Collision Detect	I	LV_CMOS 2.5V
ETHER_COMA	C1	Power Save Mode	O	LV_CMOS 2.5V
ETHER_CRS	N3	Carrier Sense	I	LV_CMOS 2.5V
ETHER_IRQ	C3	IRQ	I	LV_CMOS 2.5V
ETHER_MDC	C2	Media Independent Interface Clock	O	LV_CMOS 2.5V
ETHER_MDIO	B2	Media Independent Interface Data	I/O	LV_CMOS 2.5V
ETHER_RESET	D2	Reset	O	LV_CMOS 2.5V
ETHER_RX0	M2	MII/GMII Data In 0	I	LV_CMOS 2.5V
ETHER_RX1	M3	MII/GMII Data In 1	I	LV_CMOS 2.5V
ETHER_RX2	L2	MII/GMII Data In 2	I	LV_CMOS 2.5V
ETHER_RX3	N2	MII/GMII Data In 3	I	LV_CMOS 2.5V
ETHER_RX4	K1	MII/GMII Data In 4	I	LV_CMOS 2.5V
ETHER_RX5	P1	MII/GMII Data In 5	I	LV_CMOS 2.5V
ETHER_RX6	P2	MII/GMII Data In 6	I	LV_CMOS 2.5V
ETHER_RX7	N4	MII/GMII Data In 7	I	LV_CMOS 2.5V
ETHER_RX_CLK	L1	MII/GMII RX Clock	I	LV_CMOS 2.5V
ETHER_RX_CTL	M1	MII/GMII RX Enable	I	LV_CMOS 2.5V
ETHER_RX_ER	K3	MII/GMII RX Error	I	LV_CMOS 2.5V
ETHER_TX0	H2	MII/GMII Data Out 0	O	LV_CMOS 2.5V
ETHER_TX1	G2	MII/GMII Data Out 1	O	LV_CMOS 2.5V
ETHER_TX2	F1	MII/GMII Data Out 2	O	LV_CMOS 2.5V
ETHER_TX3	E2	MII/GMII Data Out 3	O	LV_CMOS 2.5V
ETHER_TX4	E1	MII/GMII Data Out 4	O	LV_CMOS 2.5V
ETHER_TX5	F2	MII/GMII Data Out 5	O	LV_CMOS 2.5V
ETHER_TX6	E3	MII/GMII Data Out 6	O	LV_CMOS 2.5V
ETHER_TX7	D3	MII/GMII Data Out 7	O	LV_CMOS 2.5V
ETHER_TX_CLK	K2	MII/GMII TX Clock	O	LV_CMOS 2.5V
ETHER_TX_CTL	J2	MII/GMII TX Enable	O	LV_CMOS 2.5V
ETHER_TX_ER	G1	MII/GMII TX Error	I	LV_CMOS 2.5V
FLASH_S1H_IBIY1E\	G20	8/16 Bit Mode Select	O	LV_CMOS 2.5V
FLASH_S1H_OIE\	M18	Output Enable	O	LV_CMOS 2.5V
FLASH_S1H_RIE1E1T\	B19	Reset	O	LV_CMOS 2.5V
FLASH_S1H_WME\	D18	Write Enable	O	LV_CMOS 2.5V
FLASH_S1H_WP\	A18	Write Protect	O	LV_CMOS 2.5V
FLASH_S1H_CIE\	N17	Chip Enable	O	LV_CMOS 2.5V
FLASH_A0	N18	Address 0 [LSB]	I/O	LV_CMOS 2.5V
FLASH_A1	P19	Address 1	I/O	LV_CMOS 2.5V

FLASH_A2	K18	Address 2	I/O	LV_CMOS 2.5V
FLASH_A3	J17	Address 3	I/O	LV_CMOS 2.5V
FLASH_A4	J19	Address 4	I/O	LV_CMOS 2.5V
FLASH_A5	K19	Address 5	I/O	LV_CMOS 2.5V
FLASH_A6	K17	Address 6	I/O	LV_CMOS 2.5V
FLASH_A7	G19	Address 7	I/O	LV_CMOS 2.5V
FLASH_A8	D17	Address 8	I/O	LV_CMOS 2.5V
FLASH_A9	B18	Address 9	I/O	LV_CMOS 2.5V
FLASH_A10	E19	Address 10	I/O	LV_CMOS 2.5V
FLASH_A11	F18	Address 11	I/O	LV_CMOS 2.5V
FLASH_A12	F17	Address 12	I/O	LV_CMOS 2.5V
FLASH_A13	C17	Address 13	I/O	LV_CMOS 2.5V
FLASH_A14	D19	Address 14	I/O	LV_CMOS 2.5V
FLASH_A15	G17	Address 15	I/O	LV_CMOS 2.5V
FLASH_A16	E20	Address 16	I/O	LV_CMOS 2.5V
FLASH_A17	H19	Address 17	I/O	LV_CMOS 2.5V
FLASH_A18	H18	Address 18	I/O	LV_CMOS 2.5V
FLASH_A19	F19	Address 19	I/O	LV_CMOS 2.5V
FLASH_A20	H17	Address 20	I/O	LV_CMOS 2.5V
FLASH_A21	E18	Address 21	I/O	LV_CMOS 2.5V
FLASH_A22	C19	Address 22	I/O	LV_CMOS 2.5V
FLASH_A23	C20	Address 23	I/O	LV_CMOS 2.5V
FLASH_A24	H20	Address 24	I/O	LV_CMOS 2.5V
FLASH_A25	L20	Address 25 [MSB]	I/O	LV_CMOS 2.5V
FLASH_D0	U9	Data 0 [LSB]	I/O	LV_CMOS 2.5V
FLASH_D1	V10	Data 1	I/O	LV_CMOS 2.5V
FLASH_D2	V11	Data 2	I/O	LV_CMOS 2.5V
FLASH_D3	U12	Data 3	I/O	LV_CMOS 2.5V
FLASH_D4	V8	Data 4	I/O	LV_CMOS 2.5V
FLASH_D5	V9	Data 5	I/O	LV_CMOS 2.5V
FLASH_D6	V12	Data 6	I/O	LV_CMOS 2.5V
FLASH_D7	V13	Data 7	I/O	LV_CMOS 2.5V
FLASH_D8	M19	Data 8	I/O	LV_CMOS 2.5V
FLASH_D9	M17	Data 9	I/O	LV_CMOS 2.5V
FLASH_D10	P17	Data 10	I/O	LV_CMOS 2.5V
FLASH_D11	L17	Data 11	I/O	LV_CMOS 2.5V
FLASH_D12	J18	Data 12	I/O	LV_CMOS 2.5V
FLASH_D13	K20	Data 13	I/O	LV_CMOS 2.5V
FLASH_D14	F20	Data 14	I/O	LV_CMOS 2.5V
FLASH_D15	L19	Data 15 [MSB]	I/O	LV_CMOS 2.5V
FLASH_READY	C18	Flash Status	I	LV_CMOS 2.5V
GPIO_1	B17	GPIO 1	I/O	LV_CMOS 2.5V
GPIO_2	A16	GPIO 2	I/O	LV_CMOS 2.5V
GPIO_3	B16	GPIO 3	I/O	LV_CMOS 2.5V
GPIO_4	A15	GPIO 4	I/O	LV_CMOS 2.5V
JTAG_LOOP_TCK	D12	JTAG Loop back TCK	O	LV_CMOS 2.5V
JTAG_LOOP_TDI	B12	JTAG Loop back TDI	I	LV_CMOS 2.5V
JTAG_LOOP_TDO	D13	JTAG Loop back TDO	O	LV_CMOS 2.5V
JTAG_LOOP_TMS	C16	JTAG Loop back TMS	O	LV_CMOS 2.5V
SLEEP	N19	TurboLoader Sleep Request	O	LV_CMOS 2.5V

LOAD	P20	TurboLoader Load Image Request	O	LV_CMOS 2.5V
PEEKABOO	M20	TurboLoader Send Last Address Request	O	LV_CMOS 2.5V
RAM_ICIS\	E6	Chip Select	O	LV_CMOS 2.5V
RAM_ICAIS\	B4	Column Select	O	LV_CMOS 2.5V
RAM_IRAIS\	D8	Row Select	O	LV_CMOS 2.5V
RAM_IWE\	D6	Write Enable	O	LV_CMOS 2.5V
RAM_A0	E5	Address 0 [LSB]	O	LV_CMOS 2.5V
RAM_A1	G4	Address 1	O	LV_CMOS 2.5V
RAM_A2	G5	Address 2	O	LV_CMOS 2.5V
RAM_A3	F4	Address 3	O	LV_CMOS 2.5V
RAM_A4	H16	Address 4	O	LV_CMOS 2.5V
RAM_A5	F16	Address 5	O	LV_CMOS 2.5V
RAM_A6	J16	Address 6	O	LV_CMOS 2.5V
RAM_A7	F15	Address 7	O	LV_CMOS 2.5V
RAM_A8	E15	Address 8	O	LV_CMOS 2.5V
RAM_A9	G16	Address 9	O	LV_CMOS 2.5V
RAM_A10	D5	Address 10	O	LV_CMOS 2.5V
RAM_A11	E14	Address 11	O	LV_CMOS 2.5V
RAM_A12	E16	Address 12 [MSB]	O	LV_CMOS 2.5V
RAM_BA0	D4	Bank Address 0	O	LV_CMOS 2.5V
RAM_BA1	F5	Bank Address 1	O	LV_CMOS 2.5V
RAM_CLK	D15	Clock	O	LV_CMOS 2.5V
RAM_CLKE	C13	Clock Enable [Power Save Mode]	O	LV_CMOS 2.5V
RAM_D0	A3	Data 0 (LSB)	O	LV_CMOS 2.5V
RAM_D1	A5	Data 1	I/O	LV_CMOS 2.5V
RAM_D2	A7	Data 2	I/O	LV_CMOS 2.5V
RAM_D3	A6	Data 3	I/O	LV_CMOS 2.5V
RAM_D4	B7	Data 4	I/O	LV_CMOS 2.5V
RAM_D5	B6	Data 5	I/O	LV_CMOS 2.5V
RAM_D6	C6	Data 6	I/O	LV_CMOS 2.5V
RAM_D7	B5	Data 7	I/O	LV_CMOS 2.5V
RAM_D8	B15	Data 8	I/O	LV_CMOS 2.5V
RAM_D9	B14	Data 9	I/O	LV_CMOS 2.5V
RAM_D10	C12	Data 10	I/O	LV_CMOS 2.5V
RAM_D11	B13	Data 11	I/O	LV_CMOS 2.5V
RAM_D12	A14	Data 12	I/O	LV_CMOS 2.5V
RAM_D13	A13	Data 13	I/O	LV_CMOS 2.5V
RAM_D14	A11	Data 14	I/O	LV_CMOS 2.5V
RAM_D15	C11	Data 15	I/O	LV_CMOS 2.5V
RAM_D16	H5	Data 16	I/O	LV_CMOS 2.5V
RAM_D17	H4	Data 17	I/O	LV_CMOS 2.5V
RAM_D18	J6	Data 18	I/O	LV_CMOS 2.5V
RAM_D19	J5	Data 19	I/O	LV_CMOS 2.5V
RAM_D20	M5	Data 20	I/O	LV_CMOS 2.5V
RAM_D21	L5	Data 21	I/O	LV_CMOS 2.5V
RAM_D22	M4	Data 22	I/O	LV_CMOS 2.5V
RAM_D23	K5	Data 23	I/O	LV_CMOS 2.5V
RAM_D24	V15	Data 24	I/O	LV_CMOS 2.5V
RAM_D25	T14	Data 25	I/O	LV_CMOS 2.5V
RAM_D26	P16	Data 26	I/O	LV_CMOS 2.5V

RAM_D27	K16	Data 27	I/O	LV_CMOS 2.5V
RAM_D28	N16	Data 28	I/O	LV_CMOS 2.5V
RAM_D29	L16	Data 29	I/O	LV_CMOS 2.5V
RAM_D30	M15	Data 30	I/O	LV_CMOS 2.5V
RAM_D31	J15	Data 31	I/O	LV_CMOS 2.5V
RAM_DM0-7	C8	Data Mask [0-7]	O	LV_CMOS 2.5V
RAM_DM7-15	C15	Data Mask [7-15]	O	LV_CMOS 2.5V
RAM_DM16-23	P5	Data Mask [16-23]	O	LV_CMOS 2.5V
RAM_DM24-31	M16	Data Mask [24-31]	O	LV_CMOS 2.5V

## Appendix D – CPLD Pinout

### CPLD Pinout

Net	Pin	Description	Direction
50MHZ_CLOCK	K2	50 MHz Free Running Clock Input	I
FLA\SIH\BY\T\	A7	8/16 Bit Mode Select	O
FLA\SIH\IO\	F3	Output Enable	O
FLA\SIH\RI\SI\T\	G3	Flash Reset	O
FLA\SIH\WE\	C3	Flash Write Enable	O
FLA\SIH\WP\	F1	Flash Write Protect	O
FLA\SIH\CIE\	A5	Flash Chip Enable	O
FIP\GA\PIR\IO\G\	K8	FPGA Asynchronous Reset	O
FIP\GA\PIWR\	H10	FPGA Power Save Mode	O
FLASH_A0	A4	Address 1 [8 Bit Mode]	I/O
FLASH_A1	A1	Address 2	I/O
FLASH_A2	B1	Address 3	I/O
FLASH_A3	G1	Address 4	I/O
FLASH_A4	C1	Address 5	I/O
FLASH_A5	A2	Address 6	I/O
FLASH_A6	D1	Address 7	I/O
FLASH_A7	E1	Address 8	I/O
FLASH_A8	H3	Address 9	I/O
FLASH_A9	D8	Address 10	I/O
FLASH_A10	C10	Address 11	I/O
FLASH_A11	H1	Address 12	I/O
FLASH_A12	E8	Address 13	I/O
FLASH_A13	C4	Address 14	I/O
FLASH_A14	D10	Address 15	I/O
FLASH_A15	B10	Address 16	I/O
FLASH_A16	A10	Address 17	I/O
FLASH_A17	E3	Address 18	I/O
FLASH_A18	C5	Address 19	I/O
FLASH_A19	C8	Address 20	I/O
FLASH_A20	A3	Address 21	I/O
FLASH_A21	K6	Address 22	I/O
FLASH_A22	F10	Address 23	I/O
FLASH_A23	E10	Address 24	I/O
FLASH_A24	A9	Address 25	I/O
FLASH_A25	A8	Address 26	I/O
FLASH_D15	H7	Address 0*	I/O
FPGA_CCLK	G10	FPGA Configuration Clock	O
FPGA_DONE	J1	FPGA Done Programming	I
FPGA_INIT	K1	FPGA Ready to Program	I/O
LOAD	K7	Load Image Request	I
PEEKABOO	K4	Output Last Address Before Done Request	I
SLEEP	K5	Sleep Mode Request	I

\*Pin D15 turns into Address -1 when the Flash ROM is in 8 bit mode.

## Appendix E – Standard Part Number Listing

### Standard Part Number Listing

Device	Part Number	Website
<b>PICO E-12 LO</b>		
FPGA	XC4VLX25-10SF363I*	<a href="http://www.xilinx.com/virtex4">http://www.xilinx.com/virtex4</a>
CPLD	XC2C64A-7CP56I	<a href="http://www.xilinx.com/cpld">http://www.xilinx.com/cpld</a>
RAM	K4S51163LF-YL75000	<a href="http://www.samsung.com">http://www.samsung.com</a>
ROM	S29GL512N11FAI011	<a href="http://www.amd.com/us-en/FlashMemory">http://www.amd.com/us-en/FlashMemory</a>
Ethernet	88E1111-B1-BAB-I000	<a href="http://www.marvell.com">http://www.marvell.com</a>
CF Transceivers	SN74ALVC164245KR	<a href="http://www.ti.com">http://www.ti.com</a>
<b>PICO E-12 EP</b>		
FPGA	XC4VFX12-10SF363I**	<a href="http://www.xilinx.com/virtex4">http://www.xilinx.com/virtex4</a>
CPLD	XC2C64A-7CP56I	<a href="http://www.xilinx.com/cpld">http://www.xilinx.com/cpld</a>
RAM	K4S51163LF-YL75000	<a href="http://www.samsung.com">http://www.samsung.com</a>
ROM	S29GL512N11FAI011	<a href="http://www.amd.com/us-en/FlashMemory">http://www.amd.com/us-en/FlashMemory</a>
Ethernet	88E1111-B1-BAB-I000	<a href="http://www.marvell.com">http://www.marvell.com</a>
CF Transceivers	SN74ALVC164245KR	<a href="http://www.ti.com">http://www.ti.com</a>

\*All PICO E12 LO boards that have serial numbers XXXXXXXXBES have an XC4VLX25-10SF363CES

\*All PICO E12 LO boards that have serial numbers XXXXXXXXBC have an XC4VLX25-10SF363C

\*\*All PICO E12 EP boards that have serial numbers XXXXXXXXBES have an XC4VFX12-10SF363CES

\*\*All PICO E12 EP boards that have serial numbers XXXXXXXXBC have an XC4VFX12-10SF363C

## Appendix F – Errata

The following section lists all known errata:

### **PICO E-12 LO:**

The PICO E-12 reference boards will draw excessive current before configuration [2.5W]. This conditional usually only lasts for 1/10 of a second and only occurs before and while loading FPGA images.

### **All versions:**

**Permanent damage** will result if the PICO E-12 is left un-configured and powered on for more than 10 minutes. This should not be a problem since the PICO E-12 automatically loads an FPGA image upon power-on.

**Permanent damage** will result if a strong magnetic field is exposed to the PICO for more than 10 seconds and DIAG\_EN is pulled low. This condition occurs after programming.

**Permanent damage** will result if a strong magnetic field is exposed to the PICO for more than 10 minutes and DIAG\_EN is pulled low. This condition occurs before programming.

## Appendix G – FPGA Performance Enhancements

### Overview:

Like most silicon devices, the FPGA on the PICO can be overclocked if proper cooling techniques are employed. Care must be taken to avoid thermal runaway.

### Thermal Runaway:

As the die temperature of the FPGA increases, it draws more current. This extra current gets turned into heat. If thermal equilibrium is not reached with proper cooling, the FPGA will overheat or overstress the power supplies. In all lab tests, the FPGA core power supply shut down before the FPGA could be damaged by an over temperature condition (although this behavior is not guaranteed). The maximum FPGA core temperature is 150°C. Note that chips surrounding the FPGA will be damaged by temperatures above 85°C.

### Heat Sink Placement:

The heat sink of the FPGA is internally connected via thermal grease to the case of the compact flash card on the top side (serial number side). Placing a large heat sink on the outside of the case can allow higher performance.

### Power Requirements:

To keep current consumption under the 1A maximum specified by the compact flash standard the PICO E-12 should be run at 5.0V. If an external power supply is available the board should be run at 3.3V for maximum efficiency.

### Speed Ratings:

Pico Computing uses all industrial temperature range parts where available. When a -10 industrial temperature speed grade FPGA is created, a -11 commercial speed grade part is tested to -10 performance ratings at the industrial temperature range. Pico computing does not guarantee that -10 industrial parts can be operated at -11 speeds when kept below 85°C.

## Revision History

### 3.1.4.15

Initial public release

### 3.1.6.01

Updated recommended operating temperature

Added default PCMCIA pinout

Updated FPGA pinout clock pins

### 3.1.6.02

Fixed direction of CSEL pin on PCMCIA interface

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