



**E-17**

## Hardware Technical Reference

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Hardware Revision: B



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# Product Overview:

The E-17 FPGA Card is the world's first Virtex-5 FPGA to be released in a ExpressCard/54 form factor, designed to be utilized as a co-processor for in-slot applications or as an embedded device capable of "standalone" applications.

## Interface to Host:

The E-17 has x1 PCIe lane to the host, capable of up to 2.5Gb/s bi-directional.

## Memory:

The E-17 has 256MB of DDR2

## Storage:

The E-17 has 64MB of FLASH

## I/O:

The E-17 has 32 LVDS and 4 MGT available from the I/O connector

## FPGA:

The E-17 is offered with the Virtex-5 FX70T, SX50T or LX50T:

	FX70T	SX50T	LX50T
Part Number	XC5VFX70T	XC5VSX50T	XC5VLX50T
Slices	11,200	8,160	7,200
Logic Cells	71,680	52,224	46,080
Flip-Flops	44,800	32,640	28,800
Block RAM (Kbits)	5,324	4,752	2,160
DSP48E Slices	128	288	48
PowerPC 440	1	0	0

<b>Pico Product Line</b>	<b>Form Factor</b>	<b>FPGA</b>
E-12	Compact Flash	Virtex-4 LX25/FX12
E-14	CardBus	Virtex-4 FX20/FX60
E-15	CardBus	Virtex-4 FX20/FX60
E-16	ExpressCard/34	Virtex-5 LX50
E-17	ExpressCard/54	Virtex-5 FX70T
E-101	Stand Alone	Spartan-6 LX45
EX-300	PCI Express	Spartan-3 5000
EX-160	PCI Express	E-16 Backplane

## Virtex-5 ExpressCard



### Choice of Xilinx Virtex-5 FPGA

FX70T (PowerPC 440)  
LX50T  
SX50T

### Small Form Factor

ExpressCard/54mm  
(75mm x 54mm x 5mm)

**256MB DDR2 @ 266MHz**

**64MB FLASH**

### Expansion Capabilities

32 LVDS Pairs  
4 Multi-Gigabit Transceivers



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## E-17

### Specifications

- Xilinx Virtex-5 FX70T / LX50T / SX50T
- ExpressCard/54 (75mm x 54mm x 5mm)
- 256MB DDR2
- 64MB FLASH
- 32 LVDS
- 4 MGT
- Internal JTAG for debugging
- Temperature Range: 0<sup>o</sup> to 70<sup>o</sup> C

### Applications

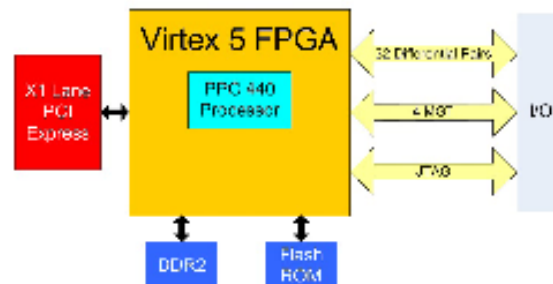
- Application On Card (AOC) systems. Applications packaged with the platform that they run on.
- Image Processing
- Algorithm Acceleration
- Hybrid embedded processor / DSP applications
- Encryption / Decryption
- Security algorithms and testing
- Software Defined Radio (SDR)
- Embedded control systems
- Weight and size constrained environments such as UAVs, surveillance systems and environmental monitoring devices
- Complete development environment for laptop computers. Ideal for rapid prototyping and classroom environments.

### Software

- PicoUtil: Utility program for FPGA management (Windows and Linux)
- Xilinx standard tool set support (ISE, EDK, and Platform SDK)
- ImpulseC CoDeveloper Platform Support Package
- Plug-in for MATLAB/Simulink available

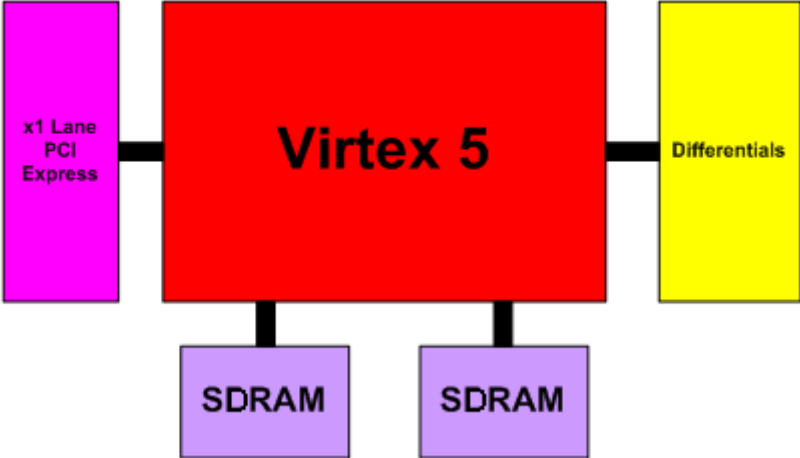
### Accessories

- E-17 Adapter Board with RS-232, Ethernet, JTAG and Header
- E-17 Standalone Board with RS-232, Ethernet, JTAG, Header, USB 2.0



# System Architecture

At the core of the Pico E-17 is a Virtex-5 FPGA. The FPGA can be dynamically configured to perform any number of specialized tasks such as: protocol processing, encryption, or complex mathematical functions.



# Pico E-17 Electrical Specifications

	Minimum	Nominal	Maximum
DC Input Voltage 3.3V	3.2V	3.3V	3.4V
DC Input Current 3.3V	0.35A	0.5A*	2A
DC Input Voltage 1.5V	1.4V	1.5V	1.6V
DC Input Current 1.5V	0.15A	0.33A*	8.5A
Power Consumption	1.5W	2W	18W
Recommended Temperature Range	°0C	°10C	°70C
Maximum Allowable Temperature Range	°0C	°10C	°70C
Maximum Storage Temperature Range	-50°C	27°C	125°C
Relative Humidity (Non-Condensing)	0%	20%	90%

\*Typical power for the SX parts is slightly lower though the maximum values stay the same.

# Peripheral I/O Connector

## Connector Information

Description	Brand	Part Number
Receptacle Stacking Connector	Samtec	QSH-060-01-L-D-A

## Peripheral I/O Connector Pinout

Name	Pin	Description	Dir	FPGA Pin
DIFFERENTIAL_0P	1	Differential or LVTTTL	I/O	E6
DIFFERENTIAL_0N	3	Differential or LVTTTL	I/O	D6
DIFFERENTIAL_1N	5	Differential or LVTTTL	I/O	C6
DIFFERENTIAL_1P	7	Differential or LVTTTL	I/O	C7
DIFFERENTIAL_2N	11	Differential or LVTTTL	I/O	E7
DIFFERENTIAL_2P	13	Differential or LVTTTL	I/O	E8
DIFFERENTIAL_3N	15	Differential or LVTTTL	I/O	D9
DIFFERENTIAL_3P	17	Differential or LVTTTL	I/O	D10
DIFFERENTIAL_4P	21	Differential or LVTTTL	I/O	G7
DIFFERENTIAL_4N	23	Differential or LVTTTL	I/O	H7
DIFFERENTIAL_5P	25	Differential or LVTTTL	I/O	H8
DIFFERENTIAL_5N	27	Differential or LVTTTL	I/O	J8
DIFFERENTIAL_6N	31	Differential or LVTTTL	I/O	B7
DIFFERENTIAL_6P	33	Differential or LVTTTL	I/O	A7
DIFFERENTIAL_7N	35	Differential or LVTTTL	I/O	D11
DIFFERENTIAL_7P	37	Differential or LVTTTL	I/O	C11
DIFFERENTIAL_8N	41	Differential or LVTTTL	I/O	C8
DIFFERENTIAL_8P	43	Differential or LVTTTL	I/O	B9
DIFFERENTIAL_9N	45	Differential or LVTTTL	I/O	A10
DIFFERENTIAL_9P	47	Differential or LVTTTL	I/O	B10
DIFFERENTIAL_10P	51	Differential or LVTTTL	I/O	B11
DIFFERENTIAL_10N	53	Differential or LVTTTL	I/O	A12
DIFFERENTIAL_11N	55	Differential or LVTTTL	I/O	A13
DIFFERENTIAL_11P	57	Differential or LVTTTL	I/O	B14
DIFFERENTIAL_12P	63	Differential or LVTTTL	I/O	A14
DIFFERENTIAL_12N	65	Differential or LVTTTL	I/O	A15
DIFFERENTIAL_13N	67	Differential or LVTTTL	I/O	A17
DIFFERENTIAL_13P	69	Differential or LVTTTL	I/O	B17
DIFFERENTIAL_14P	73	Differential or LVTTTL	I/O	G9
DIFFERENTIAL_14N	75	Differential or LVTTTL	I/O	F9
DIFFERENTIAL_15N	77	Differential or LVTTTL	I/O	D25
DIFFERENTIAL_15P	79	Differential or LVTTTL	I/O	D26
DIFFERENTIAL_16P	83	Differential or LVTTTL	I/O	C19
DIFFERENTIAL_16N	85	Differential or LVTTTL	I/O	D19
DIFFERENTIAL_17N	87	Differential or LVTTTL	I/O	C21
DIFFERENTIAL_17P	89	Differential or LVTTTL	I/O	B21
DIFFERENTIAL_18N	93	Differential or LVTTTL	I/O	D20
DIFFERENTIAL_18P	95	Differential or LVTTTL	I/O	D21
DIFFERENTIAL_19N	97	Differential or LVTTTL	I/O	C23
DIFFERENTIAL_19P	99	Differential or LVTTTL	I/O	B24
DIFFERENTIAL_20P	103	Differential or LVTTTL	I/O	A18
DIFFERENTIAL_20N	105	Differential or LVTTTL	I/O	A19
DIFFERENTIAL_21P	107	Differential or LVTTTL	I/O	A20
DIFFERENTIAL_21N	109	Differential or LVTTTL	I/O	B20

DIFFERENTIAL_22N	113	Differential or LVTTTL	I/O	A22
DIFFERENTIAL_22P	115	Differential or LVTTTL	I/O	B22
DIFFERENTIAL_23N	117	Differential or LVTTTL	I/O	A25
DIFFERENTIAL_23P	119	Differential or LVTTTL	I/O	B25
DIFFERENTIAL_24N	100	Differential or LVTTTL	I/O	C26
DIFFERENTIAL_24P	98	Differential or LVTTTL	I/O	B26
DIFFERENTIAL_25P	96	Differential or LVTTTL	I/O	D24
DIFFERENTIAL_25N	94	Differential or LVTTTL	I/O	C24
DIFFERENTIAL_26P	90	Differential or LVTTTL	I/O	B19
DIFFERENTIAL_26N	88	Differential or LVTTTL	I/O	C18
DIFFERENTIAL_27N	86	Differential or LVTTTL	I/O	C16
DIFFERENTIAL_27P	84	Differential or LVTTTL	I/O	B15
DIFFERENTIAL_28N	80	Differential or LVTTTL	I/O	C14
DIFFERENTIAL_28P	78	Differential or LVTTTL	I/O	C13
DIFFERENTIAL_29N	76	Differential or LVTTTL	I/O	C12
DIFFERENTIAL_29P	74	Differential or LVTTTL	I/O	B12
DIFFERENTIAL_30N	70	Differential or LVTTTL	I/O	D8
DIFFERENTIAL_30P	68	Differential or LVTTTL	I/O	C9
DIFFERENTIAL_31N	66	Differential or LVTTTL	I/O	F8
DIFFERENTIAL_31P	64	Differential or LVTTTL	I/O	F7
MGT_CLKN_112	18	Multi-Gigabit Transceiver Clock	I	K3
MGT_CLKP_112	16	Multi-Gigabit Transceiver Clock	I	K4
MGT_RXN0_112	60	Multi-Gigabit Transceiver Receive	I	K1
MGT_RXP0_112	58	Multi-Gigabit Transceiver Receive	I	J1
MGT_TXN0_112	28	Multi-Gigabit Transceiver Transmit	O	J2
MGT_TXP0_112	30	Multi-Gigabit Transceiver Transmit	O	H2
MGT_RXN1_112	54	Multi-Gigabit Transceiver Receive	I	L1
MGT_RXP1_112	52	Multi-Gigabit Transceiver Receive	I	M1
MGT_TXN1_112	24	Multi-Gigabit Transceiver Transmit	O	M2
MGT_TXP1_112	22	Multi-Gigabit Transceiver Transmit	O	N2
MGT_CLKN_114	4	Multi-Gigabit Transceiver Clock	I	T3
MGT_CLKP_114	6	Multi-Gigabit Transceiver Clock	I	T4
MGT_RXN0_114	46	Multi-Gigabit Transceiver Receive	I	T1
MGT_RXP0_114	48	Multi-Gigabit Transceiver Receive	I	R1
MGT_TXN0_114	10	Multi-Gigabit Transceiver Transmit	O	R2
MGT_TXP0_114	12	Multi-Gigabit Transceiver Transmit	O	P2
MGT_RXN1_114	36	Multi-Gigabit Transceiver Receive	I	U1
MGT_RXP1_114	34	Multi-Gigabit Transceiver Receive	I	V1
MGT_TXN1_114	24	Multi-Gigabit Transceiver Transmit	O	V2
MGT_TXP1_114	22	Multi-Gigabit Transceiver Transmit	O	W2
MODE0_0	61	Flash Boot Section	I	T20
TCK	108	JTAG Clock	I	V11
TDI	112	JTAG Data In	I	V13
TDO	110	JTAG Data Out	O	V12
TMS	106	JTAG Test Mode Select	I	W13
3.3V	104	3.3V Rail	Power	N/A
3.3V	118	3.3V Rail	Power	N/A
3.3V	120	3.3V Rail	Power	N/A
3.3Vaux	116	3.3V Auxiliary Rail	Power	N/A
1.5V	114	1.5V Rail	Power	N/A

### Peripheral Connector Pin #1 Location



# Express Card Connector

## Connector Information

Description	Brand	Part Number
Express Card Module Connector	WisePower	EPCN3-1005-00

## Express Card Connector Pinout

Name	Pin	Description
GND	1	Ground
USB-	2	Not Connected
USB+	3	Not Connected
CPUSB#	4	Not Connected
RESERVED	5	Not Connected
RESERVED	6	Not Connected
SMBCLK	7	Not Connected
SMBDATA	8	Not Connected
1.5V	9	1.5V
1.5V	10	1.5V
WAKE#	11	Not Connected
3.3VAUX	12	3.3VAUX
PERST#	13	PCIe Reset
3.3V	14	3.3V
3.3V	15	3.3V
CLKREQ#	16	Request that REFCLK be Enabled (Grounded on E-17)
CPPE#	17	PCIe Interface Presence Detect (Grounded on E-17)
REFCLK-	18	PCIe Reference Clock 100MHz
REFCLK+	19	PCIe Reference Clock 100MHz
GND	20	Ground
PERn0	21	PCIe x1 TX Interface
PERp0	22	PCIe x1 TX Interface
GND	23	Ground
PETn0	24	PCIe x1 RX Interface
PETp0	25	PCIe x1 RX Interface
GND	26	Ground

# Field Programmable Gate Array



The core of the Pico E-17 is a high performance Virtex-5 FPGA. Included in the FPGA are the FPGA Fabric, ultra high-speed DSP slices, and RAM.

## FPGA Fabric:

The “Fabric” of an FPGA comprises an array of logic elements that can be connected in virtually unlimited patterns. These patterns of logic elements can be used to perform basic mathematical functions such as addition and subtraction, or can be grouped together to perform complex functions like Fast Fourier Transforms. Logic elements can even be connected to create a custom soft processor.

The advantage of the FPGA is that the internal logic can be optimized for a specific application. FPGAs are also able to execute operations in parallel, not being limited by sequential execution like a traditional processor. FPGA operations can be executed in a parallel, pipelined or even an asynchronous manner. The FPGA allows incredible application speed with very low power consumption. Your imagination is really the limit.

## DSP Slice:

Embedded within the FPGA are special areas that are designed to facilitate high speed “digital signal processing.” These areas are called DSP slices. The DSP slice can be configured in a variety of different ways. For example, one DSP slice can be configured to be one tap of an FIR filter. DSP slices are fully pipelined and feature incredible speed.

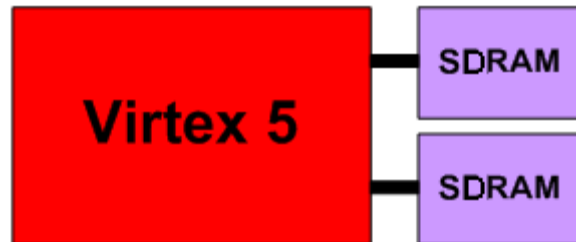
## FPGA Resources:

Free FPGA Cores	<a href="http://www.opencores.org">www.opencores.org</a>	
Encryption Cores	<a href="http://www.openciphers.org">www.openciphers.org</a>	
Virtex-5 Website	<a href="http://www.xilinx.com/virtex5">http://www.xilinx.com/virtex5</a>	

# DDR2 SDRAM Memory



The Pico E-17 comes equipped with two 1 Gb chips of DDR2 both with a 16 bit data path which are grouped into one 32 bit bank. The DDR2 can run at a maximum speed of 266MHz.



## RAM Resources:

Micron RAM Website	<a href="http://www.micron.com/products/dram/ddr2/partlist.aspx">http://www.micron.com/products/dram/ddr2/partlist.aspx</a>
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## Express Card

The Pico E-17 can run as a standalone product or can be connected to a host using the Express Card connector. By default, the Pico E-17 ships with firmware that is ready for use as an Express Card device.

The Express Card interface on the E-17 is x1 lane PCI Express. The data path consists of 2 pairs of differential signals operating at a frequency of 2.5 GHz. The theoretical bandwidth of the interface is 2.5 Gb/s full duplex. After overhead calculations (8B/10B encoding), the device is capable of a 250MBps full duplex bandwidth.

## PCMCIA Interface Resources:

Express Card Website	<a href="http://www.expresscard.org/web/site/">http://www.expresscard.org/web/site/</a>
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## Differential Interface

The E-17 features 32 pairs of general purpose differential signaling from the FPGA to the peripheral connector. The desired voltage level of operation can be set to any voltage. Once the voltage level is set the interface will be able to run at that voltage allowing greater interface to other products. These signals can also be run in single ended mode giving the user a total of 64 general purpose data lines. (Check <http://www.xilinx.com> for the most up to date information)

### Virtex-5 I/O Standards:

Virtex-5	<a href="http://www.xilinx.com/virtex5">http://www.xilinx.com/virtex5</a>
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## Multi-Gigabit Transceiver

The E-17 features 2 banks of multi-gigabit transceivers (MGTs) from the FPGA to the peripheral connector. The MGTs have the ability to operate above the rates of 1 Gigabit/second. The MGT standard uses differential signaling to allow for faster data transmission but requires a positive and negative pair for each line. The E-17 MGT banks have two RX and TX pairs as well as individual clocking for each bank allowing them to be run at \_\_\_\_\_ MHz.

# E-17 Firmware

## PCI Express

The PCIe Express core is based off of the Xilinx Endpoint Block Plus Wrapper for PCI Express. The Bus Mastering was taken from XAPP 1052, and then a wrapper was created to go from the Bus Mastering Core to the PicoBus. The PicoBus is a 32 bit bus with a read and write signal operating at 125 Mhz.

For more information on the Xilinx Endpoint:

[http://www.xilinx.com/products/ipcenter/V5\\_PCI\\_Express\\_Block\\_Plus.htm](http://www.xilinx.com/products/ipcenter/V5_PCI_Express_Block_Plus.htm)

For more information on the Bus Mastering Example:

[http://www.xilinx.com/support/documentation/application\\_notes/xapp1052.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp1052.pdf)

## Memory

There are two cores for DDR2 for the E-17:

1. PowerPC 440 DDR2 Controller:  
[http://www.xilinx.com/support/documentation/ip\\_documentation/ppc440mc\\_ddr2.pdf](http://www.xilinx.com/support/documentation/ip_documentation/ppc440mc_ddr2.pdf)
2. Multit Port Memory Controller (MPMC):  
[http://www.xilinx.com/support/documentation/ip\\_documentation/mpmc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/mpmc.pdf)

The PowerPC 440 DDR2 controller is only supported on the FX70T and can be clocked up to 266Mhz on the slowest speed grade. The MPMC is supported by both the FX70T and SX50T and can be clocked up to 200 Mhz on the slowest speed grade.

It is recommended to use the E-17 Base System Builder files to instantiate both cores.

## Base System Builder

Base System Builder files as well as tutorials on how to run through Xilinx EDK Base System Builder are available. Through Base System builder: processor, memory, Ethernet, RS-232, and GPIO can be instantiated.

## Appendix A - FPGA Pinout

Name	Pin	Description	Dir
DIFFERENTIAL_ON	E6	Differential or LVTTTL	I/O
DIFFERENTIAL_OP	D6	Differential or LVTTTL	I/O
DIFFERENTIAL_10N	B11	Differential or LVTTTL	I/O
DIFFERENTIAL_10P	A12	Differential or LVTTTL	I/O
DIFFERENTIAL_11N	A14	Differential or LVTTTL	I/O
DIFFERENTIAL_11P	B14	Differential or LVTTTL	I/O
DIFFERENTIAL_12N	A14	Differential or LVTTTL	I/O
DIFFERENTIAL_12P	F7	Differential or LVTTTL	I/O
DIFFERENTIAL_13N	A15	Differential or LVTTTL	I/O
DIFFERENTIAL_13P	F8	Differential or LVTTTL	I/O
DIFFERENTIAL_14N	A17	Differential or LVTTTL	I/O
DIFFERENTIAL_14P	C9	Differential or LVTTTL	I/O
DIFFERENTIAL_15N	B17	Differential or LVTTTL	I/O
DIFFERENTIAL_15P	D8	Differential or LVTTTL	I/O
DIFFERENTIAL_16N	F9	Differential or LVTTTL	I/O
DIFFERENTIAL_16P	B12	Differential or LVTTTL	I/O
DIFFERENTIAL_17N	G9	Differential or LVTTTL	I/O
DIFFERENTIAL_17P	C12	Differential or LVTTTL	I/O
DIFFERENTIAL_18N	D25	Differential or LVTTTL	I/O
DIFFERENTIAL_18P	C13	Differential or LVTTTL	I/O
DIFFERENTIAL_19N	D26	Differential or LVTTTL	I/O
DIFFERENTIAL_19P	C14	Differential or LVTTTL	I/O
DIFFERENTIAL_1N	C6	Differential or LVTTTL	I/O
DIFFERENTIAL_1P	C7	Differential or LVTTTL	I/O
DIFFERENTIAL_20N	C19	Differential or LVTTTL	I/O
DIFFERENTIAL_20P	B15	Differential or LVTTTL	I/O
DIFFERENTIAL_21N	D19	Differential or LVTTTL	I/O
DIFFERENTIAL_21P	C16	Differential or LVTTTL	I/O
DIFFERENTIAL_22N	C21	Differential or LVTTTL	I/O
DIFFERENTIAL_22P	C18	Differential or LVTTTL	I/O
DIFFERENTIAL_23N	B21	Differential or LVTTTL	I/O
DIFFERENTIAL_23P	B19	Differential or LVTTTL	I/O
DIFFERENTIAL_24N	D20	Differential or LVTTTL	I/O
DIFFERENTIAL_24P	C24	Differential or LVTTTL	I/O
DIFFERENTIAL_25N	D21	Differential or LVTTTL	I/O
DIFFERENTIAL_25P	D24	Differential or LVTTTL	I/O
DIFFERENTIAL_26N	C23	Differential or LVTTTL	I/O
DIFFERENTIAL_26P	D26	Differential or LVTTTL	I/O
DIFFERENTIAL_27N	B24	Differential or LVTTTL	I/O
DIFFERENTIAL_27P	C26	Differential or LVTTTL	I/O
DIFFERENTIAL_28N	A18	Differential or LVTTTL	I/O
DIFFERENTIAL_28P	A19	Differential or LVTTTL	I/O
DIFFERENTIAL_29N	A20	Differential or LVTTTL	I/O
DIFFERENTIAL_29P	B20	Differential or LVTTTL	I/O
DIFFERENTIAL_2N	E7	Differential or LVTTTL	I/O
DIFFERENTIAL_2P	E8	Differential or LVTTTL	I/O
DIFFERENTIAL_30N	A22	Differential or LVTTTL	I/O

DIFFERENTIAL_30P	B22	Differential or LVTTTL	I/O
DIFFERENTIAL_31N	A25	Differential or LVTTTL	I/O
DIFFERENTIAL_31P	B25	Differential or LVTTTL	I/O
DIFFERENTIAL_3N	D9	Differential or LVTTTL	I/O
DIFFERENTIAL_3P	D10	Differential or LVTTTL	I/O
DIFFERENTIAL_4N	G7	Differential or LVTTTL	I/O
DIFFERENTIAL_4P	H7	Differential or LVTTTL	I/O
DIFFERENTIAL_5N	H8	Differential or LVTTTL	I/O
DIFFERENTIAL_5P	J8	Differential or LVTTTL	I/O
DIFFERENTIAL_6N	B7	Differential or LVTTTL	I/O
DIFFERENTIAL_6P	A7	Differential or LVTTTL	I/O
DIFFERENTIAL_7N	D11	Differential or LVTTTL	I/O
DIFFERENTIAL_7P	C11	Differential or LVTTTL	I/O
DIFFERENTIAL_8N	C8	Differential or LVTTTL	I/O
DIFFERENTIAL_8P	B9	Differential or LVTTTL	I/O
DIFFERENTIAL_9N	A10	Differential or LVTTTL	I/O
DIFFERENTIAL_9P	B10	Differential or LVTTTL	I/O
FLASH_A0	H9	Address 0	I/O
FLASH_A1	G10	Address 1	I/O
FLASH_A2	H21	Address 2	I/O
FLASH_A3	G20	Address 3	I/O
FLASH_A4	H11	Address 4	I/O
FLASH_A5	G11	Address 5	I/O
FLASH_A6	H19	Address 6	I/O
FLASH_A7	H18	Address 7	I/O
FLASH_A8	G12	Address 8	I/O
FLASH_A9	F13	Address 9	I/O
FLASH_A10	G19	Address 10	I/O
FLASH_A11	F18	Address 11	I/O
FLASH_A12	F14	Address 12	I/O
FLASH_A13	F15	Address 13	I/O
FLASH_A14	F17	Address 14	I/O
FLASH_A15	G17	Address 15	I/O
FLASH_A16	G14	Address 16	I/O
FLASH_A17	H13	Address 17	I/O
FLASH_A18	G16	Address 18	I/O
FLASH_A19	G15	Address 19	I/O
FLASH_A20	Y18	Address 20	I/O
FLASH_A21	AA18	Address 21	I/O
FLASH_A22	Y11	Address 22	I/O
FLASH_A23	AA10	Address 23	I/O
FLASH_A24	Y10	Address 24	I/O
FLASH_A25	W11	Address 25	I/O
FLASH_BYTE#	D14	Selects Data Bus Width	I
FLASH_CE#	Y12	Chip Enable (Active Low)	I
FLASH_D0	AA15	Bidirectional Data 0	I/O
FLASH_D1	Y15	Bidirectional Data 1	I/O
FLASH_D2	W14	Bidirectional Data 2	I/O
FLASH_D3	Y13	Bidirectional Data 3	I/O
FLASH_D4	W16	Bidirectional Data 4	I/O
FLASH_D5	Y16	Bidirectional Data 5	I/O
FLASH_D6	AA14	Bidirectional Data 6	I/O
FLASH_D7	AA13	Bidirectional Data 7	I/O
FLASH_D8	AB12	Bidirectional Data 8	I/O
FLASH_D9	AC11	Bidirectional Data 9	I/O

FLASH_D10	AB20	Bidirectional Data 10	I/O
FLASH_D11	AB21	Bidirectional Data 11	I/O
FLASH_D12	AB11	Bidirectional Data 12	I/O
FLASH_D13	AB10	Bidirectional Data 13	I/O
FLASH_D14	AA20	Bidirectional Data 14	I/O
FLASH_D15	Y21	Bidirectional Data 15	I/O
FLASH_OE#	AA12	Output Enable	I
FLASH_RESET#	E15	Hardware Reset (Active Low)	I
FLASH_READY	D15	Ready Signal	O
FLASH_WE#	AA17	Write Enable (Active Low)	I
FLASH_WP#	D16	Write Protect (Active Low)	I
GPIO_VOLTAGE_POR	AF9	Power on Reset	O
GPIO_VOLTAGE_SDI	AF10	Voltage Input Control	I
MODE0_0	T20	Select Configuration Boot Sector	I
PERST#	AC19	Reset Signal on PCIe Bus	I
RAM_A0	T25	Address 0	I/O
RAM_A1	K22	Address 1	I/O
RAM_A2	U24	Address 2	I/O
RAM_A3	K25	Address 3	I/O
RAM_A4	V24	Address 4	I/O
RAM_A5	K23	Address 5	I/O
RAM_A6	T23	Address 6	I/O
RAM_A7	L24	Address 7	I/O
RAM_A8	U22	Address 8	I/O
RAM_A9	R21	Address 9	I/O
RAM_A10	J23	Address 10	I/O
RAM_A11	T22	Address 11	I/O
RAM_A12	L23	Address 12	I/O
RAM_A13	R22	Address 13	I/O
RAM_A14	L22	Address 14	I/O
RAM_A15	U21	Address 15	I/O
RAM_BA0	F23	Bank Address Input	I
RAM_BA1	M24	Bank Address Input	I
RAM_BA2	N23	Bank Address Input	I
RAM_CAS#	U25	Column Address Strobe (Active Low)	I
RAM_CK0_N	W21	Low Data Differential Clock	I
RAM_CK0_P	V21	Low Data Differential Clock	I
RAM_CK1_N	M22	High Data Differential Clock	I
RAM_CK1_P	N22	High Data Differential Clock	I
RAM_CKE	F25	Clock Enable	I
RAM_CS#	V23	Chip Select (Active Low)	I
RAM_D0	Y22	Bidirectional Data 0	I/O
RAM_D1	P23	Bidirectional Data 1	I/O
RAM_D2	AA23	Bidirectional Data 2	I/O
RAM_D3	T24	Bidirectional Data 3	I/O
RAM_D4	R23	Bidirectional Data 4	I/O
RAM_D5	AB24	Bidirectional Data 5	I/O
RAM_D6	P21	Bidirectional Data 6	I/O
RAM_D7	AA22	Bidirectional Data 7	I/O
RAM_D8	AB26	Bidirectional Data 8	I/O
RAM_D9	R26	Bidirectional Data 9	I/O
RAM_D10	W24	Bidirectional Data 10	I/O
RAM_D11	U26	Bidirectional Data 11	I/O
RAM_D12	R25	Bidirectional Data 12	I/O
RAM_D13	AA25	Bidirectional Data 13	I/O

RAM_D14	P25	Bidirectional Data 14	I/O
RAM_D15	AB25	Bidirectional Data 15	I/O
RAM_D16	H23	Bidirectional Data 16	I/O
RAM_D17	E25	Bidirectional Data 17	I/O
RAM_D18	K26	Bidirectional Data 18	I/O
RAM_D19	G22	Bidirectional Data 19	I/O
RAM_D20	F22	Bidirectional Data 20	I/O
RAM_D21	H22	Bidirectional Data 21	I/O
RAM_D22	E23	Bidirectional Data 22	I/O
RAM_D23	M25	Bidirectional Data 23	I/O
RAM_D24	N24	Bidirectional Data 24	I/O
RAM_D25	G26	Bidirectional Data 25	I/O
RAM_D26	J26	Bidirectional Data 26	I/O
RAM_D27	J25	Bidirectional Data 27	I/O
RAM_D28	H26	Bidirectional Data 28	I/O
RAM_D29	M26	Bidirectional Data 29	I/O
RAM_D30	G25	Bidirectional Data 30	I/O
RAM_D31	N26	Bidirectional Data 31	I/O
RAM_DM0_7	P24	Input Data Mask	I
RAM_DM16_23	G24	Input Data Mask	I
RAM_DM24_31	E26	Input Data Mask	I
RAM_DM8_15	P26	Input Data Mask	I
RAM_DQS0_N	W23	Data Strobe for Lower Byte	I/O
RAM_DQS0_P	Y23	Data Strobe for Lower Byte	I/O
RAM_DQS1_N	W25	Data Strobe for Upper Byte	I/O
RAM_DQS1_P	W26	Data Strobe for Upper Byte	I/O
RAM_DQS2_N	K21	Data Strobe for Lower Byte	I/O
RAM_DQS2_P	J21	Data Strobe for Lower Byte	I/O
RAM_DQS3_N	N21	Data Strobe for Upper Byte	I/O
RAM_DQS3_P	M21	Data Strobe for Upper Byte	I/O
RAM_RAS#	V22	Row Address Strobe (Active Low)	I
RAM_WE#	F24	Write Enable (Active Low)	I
TCK	V11	JTAG Clock	I
TDI	V13	JTAG Data In	I
TDO	V12	JTAG Data Out	O
TMS	W13	JTAG Test Mode Select	I
MGT_CLKN_112	K3	Multi-Gigabit Transceiver Clock	I
MGT_CLKP_112	K4	Multi-Gigabit Transceiver Clock	I
MGT_RXN0_112	K1	Multi-Gigabit Transceiver Receive	I
MGT_RXP0_112	J1	Multi-Gigabit Transceiver Receive	I
MGT_RXN1_112	L1	Multi-Gigabit Transceiver Transmit	O
MGT_RXP1_112	M1	Multi-Gigabit Transceiver Transmit	O
MGT_TXN0_112	J2	Multi-Gigabit Transceiver Receive	I
MGT_TXP0_112	H2	Multi-Gigabit Transceiver Receive	I
MGT_TXN1_112	M2	Multi-Gigabit Transceiver Transmit	O
MGT_TXP1_112	N2	Multi-Gigabit Transceiver Transmit	O
MGT_CLKN_114	T3	Multi-Gigabit Transceiver Clock	I
MGT_CLKP_114	T4	Multi-Gigabit Transceiver Clock	I
MGT_RXN0_114	T1	Multi-Gigabit Transceiver Receive	I
MGT_RXP0_114	R1	Multi-Gigabit Transceiver Receive	I
MGT_RXN1_114	U1	Multi-Gigabit Transceiver Transmit	O
MGT_RXP1_114	V1	Multi-Gigabit Transceiver Transmit	O
MGT_TXN0_114	R2	Multi-Gigabit Transceiver Receive	I
MGT_TXP0_114	P2	Multi-Gigabit Transceiver Receive	I
MGT_TXN1_114	V2	Multi-Gigabit Transceiver Transmit	O

## Appendix B - Standard Part Number Listing

### Standard Part Number Listing

Device	Part Number	Website
<b>Pico E-17</b>		
Virtex-5	XC5VFX70T	<a href="http://www.xilinx.com/">http://www.xilinx.com/</a>
Micron SDRAM	MT47H64M16HR-3	<a href="http://www.micron.com/products/dram/ddr2/partlist.aspx">http://www.micron.com/products/dram/ddr2/partlist.aspx</a>

## Appendix C - Errata

The following section lists all known errata:

# Appendix D - FPGA Performance Enhancements

## **Overview:**

Like most silicon devices, the FPGA on the Pico can be overclocked if proper cooling techniques are employed. Care must be taken to avoid thermal runaway.

## **Thermal Runaway:**

As the die temperature of the FPGA increases, it draws more current. This extra current gets turned into heat. If thermal equilibrium is not reached with proper cooling, the FPGA will overheat or overstress the power supplies.

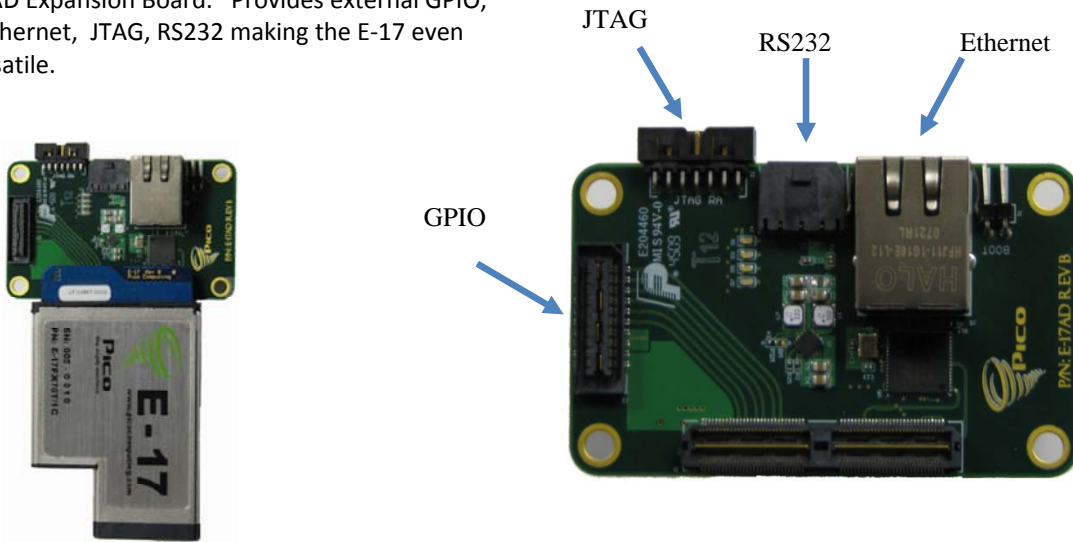
## **Heat Sink Placement:**

The heat sink of the FPGA is internally connected via thermal grease to the case of the express card on the top side (serial number side). Placing a large heat sink on the outside of the case can allow higher performance.

# Appendix E – E-17 Accessories

## E-17AD Expansion Board

The E-17AD Expansion Board. Provides external GPIO, one 1G Ethernet, JTAG, RS232 making the E-17 even more versatile.



## GPIO Pin Out

Signal Name	GPIO Pin	FPGA Ball
GPIO_6P	1	F9
GPIO_0P	2	B12
GPIO_6N	3	G9
GPIO_0N	4	C12
GPIO_7N	5	D25
GPIO_1P	6	C13
GPIO_7P	7	D26
GPIO_1N	8	C14
GPIO_8P	9	C19
GPIO_2P	10	B15
GPIO_8N	11	D19
GPIO_2N	12	C16
GPIO_9N	13	C21
GPIO_3N	14	C18
GPIO_9P	15	B21
GPIO_3P	16	B19
GPIO_10N	17	D20
GPIO_4N	18	C24
GPIO_10P	19	D21
GPIO_4P	20	D24
GPIO_11N	21	C23
GPIO_5P	22	B26
GPIO_11P	23	B24
GPIO_5N	24	C26

GPIO_12P	25	A18
GND	26	-
GPIO_12N	27	A19
2.5V	28	-
GPIO_13P	29	A20
GND	30	-
GPIO_13N	31	B20
2.5V	32	-
GPIO_14N	33	A22
GND	34	-
GPIO_14P	35	B22
3.3V	36	-
GPIO_15N	37	A25
GND	38	-
GPIO_15P	39	B25
3.3V	40	

# Revision History

## **1.00.00.00**

Draft release

## **1.00.00.01**

Expansion of Standalone Information, MGT Documentation Added

## **1.00.00.02**

Power Information added, Peripheral Connector pin out updated, Accessories and Firmware added.

## Legal Notices

### FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at their own expense.

### CE Class A

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

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